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10/699,909	11/03/2003	Jason Harold Culler	200310794-1	5350

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EXAMINER	
RAHMAN, FAHMIDA	

ART UNIT	PAPER NUMBER
2116	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/699,909	CULLER, JASON HAROLD	
	Examiner	Art Unit	
	Fahmida Rahman	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 May 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15,18 and 20-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15,18 and 20-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This final action is in response to communications filed on 5/30/2007.

2. Claims 1, 25, 30 and 36 have been amended, and claims 16-17, 19 have been cancelled. Thus, claims 1-15, 18, 20-38 are pending.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 25, 26, 30 are rejected under 35 U.S.C. 102(e) as being anticipated by Bi et al (US Patent Application Publication 2003/0052662)

For claim 1, Bi et al teach the following limitations:

A system comprising:

a sample network (Fig 4) **that provides plural samples** (211, 221) **of an input signal state** (201) **for different time instances of the input signal** (201 at time t-T, 211 correspond to t, 221 corresponds to t+T are sampled in part of detector 230 and 240), **each of the plural samples corresponding to the input signal delayed by a known amount of time** (201 correspond to t-T, 221 correspond to t+ T, 211 corresponds to t.

Therefore, these samples represent input signal delayed by known amount of time); **and a detector** (230, 240, 250, 260, 270, 280, 290) **that determines the frequency for the input signal** ([0040]) **based on samples of the input signal state received by the detector for different time instances of the input signal residing within one period of the input signal** (the input samples at t, t-T, t+T resides within one period of yt. [0010] discussed the background work that refers Ishikawa (US Pat 5444416). Ishikawa shows details of how samples are collected. Fig 3 shows that these samples are collected over one period of yt. These are received by part of detector 230 and 240 of Bi), **and the known amount of time for each of the plural samples** (T is the known amount of delay that is used in equation as shown in [0023]), **the detector provides a value that represents the determined frequency of the input signal** ([0040]).

For claims 25 and 30, Bi et al teach the following limitations:

A frequency detection system comprising:

means for sampling (Fig 4) **an input signal** (201) **having an unknown frequency** (the system determines the frequency of the FM modulated signals as explained in abstract) **and for providing plural indications of signal state** (yt, yt-T, yt+T as shown in [0021]) **associated with different time instances of the input signal delayed for different amounts of time** (210 delays 201 to produce yt, 220 delays 211 to produce yt+T. Therefore, 230 receives two inputs: 221, which represents yt+T, a delayed signal by 2T as shown in Fig 4, and 221, which represents yt-T, undelayed signal. 240 receives 211, which represents yt, a delayed signal by T as shown in Fig 4. Therefore,

signals different time instances of input signals are delayed by different amounts of time); **and means for determining** (230, 240, 250, 260, 270, 280, 290) **a frequency for the input signal** ([0021]) **based on I) the plural indications of signal state received by the means for determining, that correspond to time instances of the input signal residing within a single period of the input signal and ii) the known amounts of time** (the input samples at t, t-T, t+T resides within one period of yt. [0010] discussed the background work that refers Ishikawa (US Pat 5444416). Ishikawa shows details of how samples are collected. Fig 3 of Ishikawa shows that these samples are collected over one period of yt. These are received by part of means of determining 230 and 240. Frequency determination depends on collecting samples delayed by the known amounts of time); **and means for providing a corresponding frequency value for the determined frequency** (Fig 4).

For claim 26, delaying means are selected parts of sampling means.

4. Claim 15 is ejected under 35 U.S.C. 102(e) as being anticipated by Majos (US Patent 6701445).

A system comprising:

a plurality of storage elements (14, 15, 16, 17 of Fig 2), the plurality of storage elements being clocked to latch (Fig 2) different time instances of an input signal (1H in Fig 2) to provide corresponding output samples of the input signal (Q1(Tn), Q2 (Tn-k),

Q3(Tn+dt), Q4(Tn-k+dt) of Fig 2) sufficient for determining a frequency value (H+, H-) of the input signal (3 determines frequency value H+, H- from Q1-Q4);

a plurality of delay elements (11, 12) associated with at least a substantial number of the storage elements (11-12 are associated with 14-17, each of the delay elements delaying a sample signal (1E) by a respective known amount of time (R1 is defined and dt is predetermined; lines 20-45 of column 5) to provide a respective clock signal (Fig 2) that clocks a respective one of the at least a substantial number of the storage elements (clock signals clock 14-17 in Fig 2) to latch a respective one of the different time instances of the input signal (the different instances of input signal is latched as shown in Fig 2) to provide at least a portion of the corresponding output samples (Fig 2); and a detector (3) that provides a frequency value (H+, H-) for the input signal (combination of H+, H- is a frequency value for the input signal as the combination provides indication of frequency of H as explained in table of column 7) based (i) on output samples that correspond to different time instances of the input signal (Q1-Q4 are input to 3 as shown in Fig 1) and (ii) the known amount of time for each respective delay element (samples are dependent on the R1 and dt time. If R1 is not chosen properly, the width of clock signal can be zero and the samples may not be produced. Q3 and Q4 are directly related dt as shown in Fig 2. As samples are based on R1 and dt and 3 provides frequency value based on samples, the detector provides frequency value based on output samples and the known amount of time).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2-9, 11, 27, 28, 31-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bi et al (US Patent Application Publication 2003/0052662), in view of Lee et al (US Patent 6326826).

For claims 2-3, 31-33, Bi et al do not teach plurality of storage elements. Lee et al teach plural storage elements (22') to provide samples (EDGE[N]) corresponding to plural samples of REF_CK at the output of delay elements. The system of Lee et al further comprises delay elements (Delay0-Delay6) for delayed clock signal (CK[N]) to clock storage 22' to sample input signal at different time interval (the plural samples of input signal just at the end of delay elements are sampled at different time interval) and thereby providing plural samples of the input signal state to the decision logic 23.

It would have been obvious for one ordinary skill in the art at the time the invention was made to combine the teachings of Bi et al and Lee et al. One ordinary skill would be motivated to use storage elements with delay elements when sequential design is preffered.

For claim 4, input signal REF_CK is delayed by delay elements.

For claims 5 and 6, clock signal activates the storage elements in Fig 2 of Lee. However, neither Bi nor Lee teaches that the oscillator generates the clock signal that is activating the storage.

Examiner takes an official notice that the oscillator generating clock signal is well known in the art. An ordinary skill in the art would have been motivated to have an oscillator providing the clock signal REF_CK, since oscillator provides an on-chip generation of clock signal. The oscillator generated signal is divided by PLL and therefore, oscillator generated clock typically has higher frequency that the supplied clock.

For claims 7, Lee et al teach 7 storage elements (22') to provide samples (EDGE[N]) corresponding to plural samples of REF_CK at the output of 7 delay elements. The system of Lee et al further comprises delay elements (Delay0-Delay6) with fixed known amount of delay for delayed clock signal (CK[N]) to clock storage 22' to sample input signal at different time interval (the plural samples of input signal just at the end of delay elements are sampled at different time interval) and thereby providing plural samples of the input signal state to the decision logic 23.

For claim 8, delay components are in series. The oscillator can be used to generate a clock from which REF_CK can be generated.

For claim 9, note Fig 1.

For claim 11, Lee provides the plural storage to latch samples concurrently (i.e., within one period) to the detector.

For claims 27 and 28, Bi et al do not teach any clock signal. Lee teaches delaying clock signal (Fig 1) to provide activation signal to control sampling and plural means of storing signal (Fig 2).

It would have been obvious for one ordinary skill in the art at the time the invention was made to combine the teachings of Bi et al and Lee et al. One ordinary skill would be motivated to use storage elements with delay elements when sequential design is preferred.

For claims 34 and 35, Lee et al provides clock to control activation and delays propagation of signal through the plural storage elements having known amount of delay to establish the time intervals (Fig 1 and Fig 2).

6. Claims 10 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bi et al (US Patent Application Publication 2003/0052662), further in view of Lee et al (US Patent 6326826), further in view of Majos (US Patent 6701445).

For claims 10 and 29, neither Bi et al nor Lee et al teach that the input signal is directly connected to storage. Majos teaches that the input H is directly connected to the plurality of storage. One ordinary skill would be motivated to connect the input directly to the plural storage as that would provide a faster design.

7. Claims 12, 13, 36, 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bi et al (US Patent Application Publication 2003/0052662), in view of in view of Majos (US Patent 6701445).

For claims 12, 13, 36 and 37, Bi et al do teach any comparator. Majos teaches a comparator (3) that provides comparison signal (H+ and H-) based comparing desired value (frequency of Din) and actual value (frequency of H). 4 and 5 are the controller that adjusts the clock signal based on comparator signal.

It would have been obvious for one ordinary skill in the art at the time the invention was made to combine the teachings of Bi et al and Majos. One ordinary skill would be motivated to adjust the clock signal to get synchronized with data.

8. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bi et al (US Patent Application Publication 2003/0052662).

Bi et al do not explicitly mention about IC chip. Examiner takes an official notice that the system implemented within the IC chip is well known in the art. An ordinary skill in the art would have been motivated to implement the system within the IC chip for many reasons, such as, to make commercially available to the customers. Bi et al addressed the practicability for implementation in hardware ([0013]). Therefore, the system can be adapted to an IC chip.

9. Claims 18, 21-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Majos (US Patent 6701445), in view of Lee et al (US Patent 6326826).

For claim 18, Majos teaches the plurality of delay elements (R1, dt) to provide the respective delayed clock signals (clock to 14-15 has 0 delay, clock to 16-17 has dt delay) for clocking the at least a substantial number of the storage elements to latch the different time instances of the input signal into the storage elements (Fig 2). Majos does not teach that the input signal comprises the sample signal and the input signal being delayed by the plurality of delay elements.

Lee et al teach input signal comprises sample signal, the input signal delayed by delay elements (Fig 1).

It would have been obvious for one ordinary skill in the art to combine the teachings of Majos and Lee. One ordinary skill would be motivated to have the input signal comprises the delay signal depending on his design criterion.

For claim 21, Lee et al teach that the delay elements (18') provide respective clock edges (CK[1:7] in Fig 2) for activating the storage elements (22'), each of the clock edges corresponding to a different delayed version of the clock signal (11).

For claim 22, the delay elements in 11 of Lee et al are connected in series.

For claim 23, Majos teaches that the input H is directly connected to the plurality of storage.

For claim 24, 14-15 of Majos are clocked at an interval "0" and 16-17 are clocked at interval "dt" to latch the output samples to the detector concurrently.

10. Claims 20 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Majos (US Patent 6701445).

For claim 20, lines 60-62 of Majos mention that sample signal is a clock signal. However, it does not mention oscillator.

Examiner takes an official notice that the oscillator generating clock signal is well known in the art. An ordinary skill in the art would have been motivated to have an oscillator providing the clock signal, since oscillator provides an on-chip generation of clock signal.

For claim 38, H+ and H- are not expressed in unit of inverse of period. However, system of Majos provides corrected frequency Hout from H+ and H-, which is in unit of inverse of a period of the input signal.

Response to Arguments

Applicant's arguments with respect to claim 1-15, 18, 20-38 have been considered but are moot in view of the new ground(s) of rejection.

Applicant argues that Bi does not receive samples of an input signal state for different instances of the input signal. Instead, the inverse cosine computing means disclosed in Bi only receives one incremented signal at. Accordingly Bi fails to disclose each and every element of amended claim 1.

Examiner disagrees. The incremented signal st is based on three consecutive samples yt-T, yt and yt+T ([0023]-[0024]), which are on 201, 221 and 211. 230 multiplies yt-T and yt+T and 240 multiplies yt with yt. The results of multiplication are combined in 250. All these steps are required to compute frequency of the input signal. Thus, detector

(combination of 230, 240, 250, 260, 270, 280, 290) computes frequency based on samples yt-T, yt and yt+T. 230 and 240 receives samples of an input signal state for different time instances of the input signal.

Applicant further argues that Majos does not disclose a plurality of delay elements as recited in claim 15. The output of time delay R1 11 is provided to an XOR gate 10 and time delay R1 11 does not provide a clock signal that clocks a storage element.

Examiner disagrees. Lines 1-5 of column 5 mention that clock inputs of FF 14 and 15 are connected to the output of XOR 10. Thus, output of R1 11 is provided to the clock input of the FFs through 10. Delay R11 defines the width of sampling pulse (i.e., clock), which commands storing of H in 14 to 17. Thus, R1 11 delays sample signal 1E to provide the appropriate clock pulse to the FFs 14 and 15 to clock the FFs through XOR gate 10.

Applicant further argues that signal H is not provided to each of the storages directly in Majos as H is not provided to 15 and 17 directly.

Examiner disagrees. There is no requirement that each FF needs to be considered one single storage. 14 and 15 comprise one storage, and 16 and 17 comprise another storage. Thus, H is provided to each of the plurality of storages directly. Such a design can be practiced in sequential circuit like Majos did.

Applicant further argues that nothing in Majos teaches or suggests that the disclosed frequency comparator 3 compares two frequency values (a desired and an actual), in contrast to the comparator recited in claim 12.

Examiner disagrees. Table in column 7 provides H+ and H- as the comparison signal. This comparison signal is provided based on the decision (i.e., "H too fast", "H too slow" etc) shown in table. Such decision is based on comparison of two frequency values (note lines 5-20 of column 7 that mentions "H too fast" implies period of H contained in period of Din). Thus, when frequency value of H is faster compared to the frequency value of Din, H- and H+ becomes 1 and 0.

Applicant further argues that Hout is a recovered clock signal and is not a frequency value. Accordingly, H cannot correspond to the frequency recited in claim 38, where frequency value is expressed in units of an inverse of a period of an input signal.

Examiner agrees that Hout is a recovered signal. However, the frequency value of this recovered signal can be determined easily. Lines 19-21 of column 3 mention that the outgoing clock signal is the recovered clock signal originally produced by the transmitter. Typically the frequency of the clock signal of the transmitter is known and therefore, frequency value of Hout is typically known. Besides H's frequency is set to be equal to frequency of Din when H+=0 H-=0. In such a case, frequency value H+H-

represents frequency of H in units of inverse of period, as frequency of Din can be known to the system. Therefore, it is obvious to figure out the frequency of H from H+H- (i.e., when H+H- = 00) as frequency of Din can be known.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fahmida Rahman whose telephone number is 571-272-8159. The examiner can normally be reached on Monday through Friday 8:30 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number

for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Fahmida Rahman
Examiner
Art Unit 2116

THUAN N. DU
PRIMARY EXAMINER